In the Claims

Applicants have submitted a new complete claim set with insertions indicated by underlining and deletions indicated by strikethrough and/or double bracketing. Please amend the claims as shown below:

1. (Currently amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the at least one processor and debug circuit; ~~and~~

a communication link coupling the at least one processor and debug circuit, wherein the at least one processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the at least one processor;

wherein the program counter value has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the at least one processor; and

wherein the at least one processor is further configured to transmit to the debug circuit a status indicating that a computer instruction [[is]] in the writeback stage is a valid computer instruction.

2. (Canceled)

3. (Canceled)

4. (Currently amended) The microcomputer according to claim [[3]] 1, wherein the at least one processor is further configured to transmit to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

5. (Canceled)

6. (Currently amended) The microcomputer according to claim 1, wherein the at least one processor is further configured to transmit to the debug circuit a process identifier value.

7. (Currently amended) The microcomputer according to claim 1, wherein the at least one processor is further configured to transmit to the debug circuit a signal indicating that a current process identifier value differs from a process identifier value of a previously-executed instruction.

8. (Currently amended) The microcomputer according to claim 1, wherein the debug circuit is configured to store the program counter of the at least one processor in a memory-mapped register.

9. (Currently amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the at least one processor and debug circuit; and

a communication link coupling the at least one processor and debug circuit, wherein the at least one processor is configured to transmit to the debug circuit through the communication link in real time, a program counter value indicating the program counter of the at least one processor;

~~The microcomputer according to claim 1,~~ wherein the debug circuit is adapted to generate trace information including the program counter.

10. (Canceled)

11. (Currently amended) The microcomputer according to claim [[5]] 1, wherein the at least one processor is further configured to transmit to the debug circuit a value indicating the program counter of the at least one processor has incremented; and

~~The microcomputer according to claim 1,~~ wherein the at least one processor is further configured to transmit to the debug circuit a value indicating an amount by which the program counter is incremented.

12. (Currently amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the at least one processor and debug circuit; ~~and~~

means for transmitting to the debug circuit in real time, a program counter value indicating the program counter of the at least one processor;

wherein the program value counter has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the at least one processor; and

wherein the at least one processor includes means for transmitting to the debug circuit a status indicating that a computer instruction [[is]] in the writeback stage is a valid computer instruction.

13. (Canceled)

14. (Canceled)

15. (Currently amended) The microcomputer according to claim [[14]] 12, wherein the at least one processor includes means for transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

16. (Canceled)

17. (Currently amended) The microcomputer according to claim 12, wherein the at least one processor includes means for transmitting to the debug circuit a process identifier value.

18. (Currently amended) The microcomputer according to claim 12, wherein the at least one processor includes means for transmitting to the debug circuit [[an]] a signal indicating that a current process identifier value differs from a processor identifier value of a previously-executed instruction.

19. (Currently amended) The microcomputer according to claim 12, wherein the debug circuit includes means for storing the program counter of the at least one processor in a memory-mapped register.

20. (Currently amended) A microcomputer comprising:

at least one processor;

a debug circuit, wherein the at least one processor and debug circuit are implemented on a same integrated circuit;

a system bus coupling the at least one processor and debug circuit; ~~and~~

means for transmitting to the debug circuit in real time, a program counter value indicating the program counter of the at least one processor;

~~The microcomputer according to claim 12,~~ wherein the debug circuit includes means for generating trace information including the program counter.

21. (Canceled)

22. (Currently amended) The microcomputer according to claim [[16]] 12, wherein the at least one processor includes means for transmitting to the debug circuit a value indicating the program counter of the at least one processor has incremented; and

wherein the at least one processor includes means for transmitting to the debug circuit a value indicating an amount by which the program counter is incremented.

23. (Currently amended) A method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of:

transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor;

wherein the program counter value has a value corresponding to a value of the program counter at a writeback stage of a pipeline of the processor;

the method further comprising a step of transmitting to the debug circuit a status indicating that a computer instruction [[is]] in the writeback stage is a valid computer instruction.

24. (Canceled)

25. (Canceled)

26. (Currently amended) The method according to claim [[25]] 23, the method further comprising a step of transmitting to the debug circuit a status indicating that the computer instruction in the writeback stage is a first instruction past a branch instruction.

27. (Canceled)

28. (Original) The method according to claim 23, the method further comprising a step of transmitting to the debug circuit a process identifier value.

29. (Currently amended) The method according to claim 23, the method further comprising a step of transmitting to the debug circuit [[an]] a signal indicating that a current

process identifier value differs from a processor identifier value of a previously-executed instruction.

30. (Original) The method according to claim 23, the method further comprising a step of storing the program counter of the processor in a memory-mapped register of the debug circuit.

31. (Currently amended) A method for transferring information between a processor and a debug circuit of a microcomputer, the processor and debug circuit being implemented on a same integrated circuit, the method comprising steps of:

transmitting, in real time to the debug circuit on a communication link coupling the processor and the debug circuit, a program counter value indicating the program counter of the processor;

~~The method according to claim 23,~~ the method further comprising a step ~~of~~ whereby the debug circuit ~~generating~~ generates trace information including the program counter.

32. (Canceled)

33. (Currently amended) The method according to claim [[27]] 23, the method further comprising a step of transmitting to the debug circuit a value indicating the program counter of the processor has incremented; and

the method further comprising a step of incrementing the program counter by a value depending upon a mode signal.

34. (Previously Added) The microcomputer according to claim 8, wherein the debug circuit includes the memory-mapped register.

35. (Previously Added) The microcomputer according to claim 19, wherein the debug circuit includes the memory-mapped register.

36. (Previously Added) The microcomputer according to claim 30, wherein the debug circuit includes the memory-mapped register.